**Cell Description:**This is a standard 2 input multiplexor with an inverted output cell described by the following Boolean equation.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S** | **A** | **B** | **Y** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "MUXINV2x1" "behavioral"

module MUXINV2X1( Y, A, B, S );

input A;

input S;

output Y;

input B;

assign Y = ~((~S&A) | (S&B));

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(S => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| MUXINV2X1 | 27.0 | 14.4 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.331604 | 4.139029 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.33067 | 3.905376 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.248249 | 3.015543 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| MUXINV2X1 | 0.275295 | 3.230027 |

**Logic Symbol:**

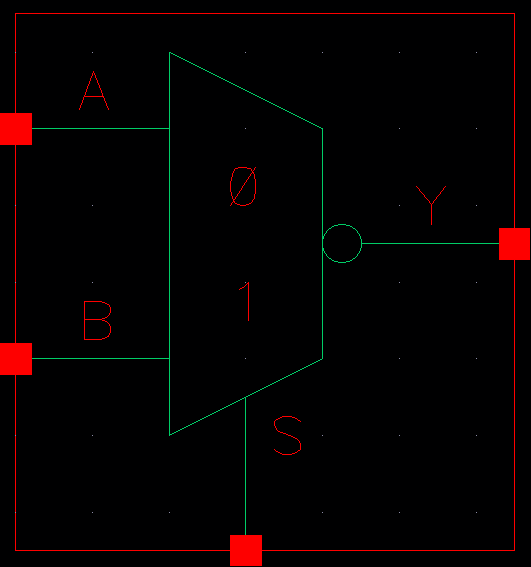
****

Figure 1: Symbol View for the MUXINV cell.

**CMOS Schematic:**

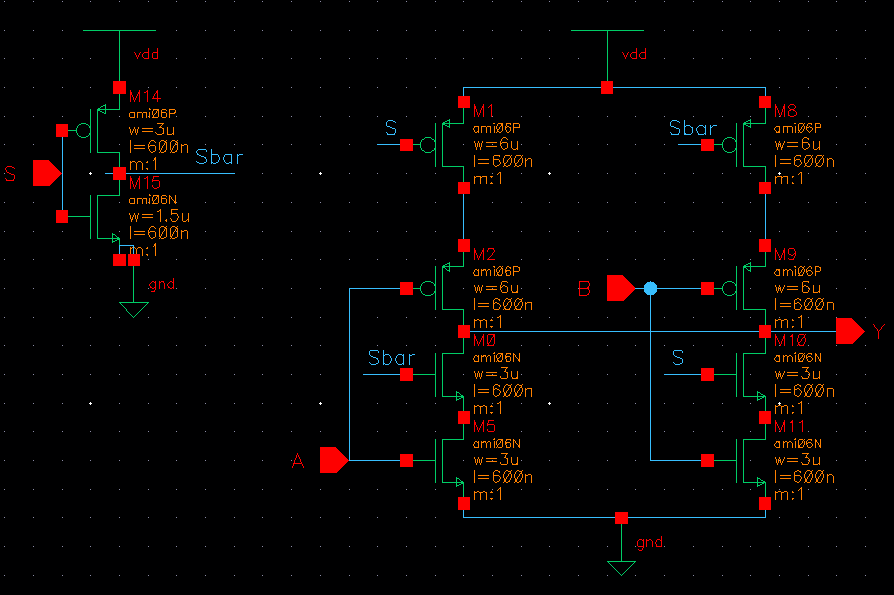
****

Figure 2: CMOS Schematic for the MUXINV2X1 cell.

**CMOS Layout:**

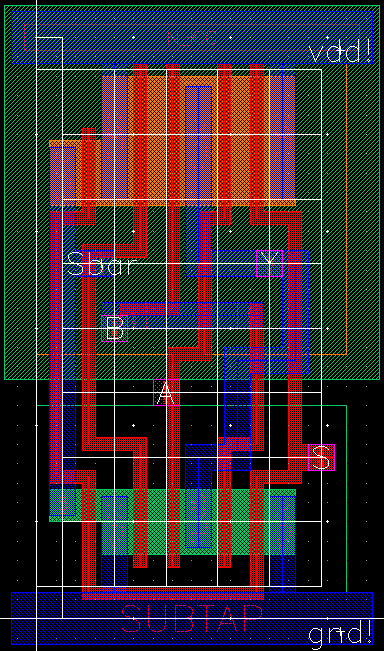
****

Figure 3: CMOS layout for the MUXINV2X1 cell.